Appl. No. 10/665,880
Amdt. dated June 17, 2009
Reply to Office Action of April 17, 2009

PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-3. (Canceled)

4.   (Currently amended) A method for generating timing constraints, comprising the steps of:

describing a digital circuit using a hardware description language (HDL);

preparing a digital circuit representation from said HDL description;

removing flip-flops from said digital circuit representation **using a computer;** ~~and~~

replacing said removed flip-flops with negative delay elements; and

breaking any feedback paths in the digital circuit representation by inserting dummy flip-flops clocked by clocks having a prescribed period.

5.   (Previously presented)   The method of Claim 4, wherein said negative delay elements are implemented by buffers having a delay -T, where T is a delay equal to a flip-flop's clock period less a predetermined flip-flop delay.

6. (Canceled)

7.   (Previously presented)   The method of Claim 4, where said step of breaking said feedback paths includes determining if said feedback paths can be broken without breaking any feedforward paths, where the breaking operation is conducted so as to maintain feedforward paths except where said determining operation answers in the negative.

Appl. No. 10/665,880
Amdt. dated June 17, 2009
Reply to Office Action of April 17, 2009

PATENT

8.   (Previously presented)   The method of Claim 4, where said replacing step is conduced so that predetermined optimization goals at each gate are substantially the same as they would be if registers were already optimally distributed.

9.   (Previously presented)   The method of Claim 5, wherein T is set to a clock period of a flip-flop being replaced.

10.   (Currently amended)   A method for generating timing constraints, comprising the steps of:

describing a digital circuit using a hardware description language (HDL);

preparing a digital circuit representation from said HDL description;

removing flip-flops from said digital circuit representation **using a computer;** ~~and~~

replacing said removed flip-flops with negative delay elements; and

where some of the negative delay elements comprise buffers, said buffers having a load capacitance representing an average or weighted-average load capacitance taken over inputs of all gates and flip-flop D pins in a target technology library.

11.   (Currently amended)   A method for generating timing constraints, comprising operations of:

describing a digital circuit using a hardware description language (HDL);

preparing a digital circuit representation from said HDL description;

replacing flip-flops in said digital circuit representation with negative delay elements **using a computer**;

wherein said negative-time elements are implemented by buffers having a delay -T, where T is a delay equal to a flip-flop's clock period less a predetermined flip-flop delay;

describing a value of T using a capacitance/delay curve representing a composite of gates in a target technology library, Q pins of flip-flops in said target technology library, and a series of increasingly powerful buffer trees;

wherein said curve is first computed, then it is offset by setting a delay corresponding to a predetermined load capacitance to -T;

whereby a larger capacitive load results in a longer delay; and

whereby if a near-zero load is imposed a delay is -(T + t), where t is a (positive) difference in delay between a predetermined load and a lesser load.

12.   (Previously presented)   The method of Claim 4, further comprising the steps of:

after said replacing and breaking steps, optimizing logic of said digital circuit representation;

after said optimizing, reinstalling registers in place of said negative-delay elements and removing all dummy flip-flops;

applying a retiming process to reposition registers to optimize timing slack and register count while preserving the optimized logic, said operation of applying the retiming process producing a retimed design; and

after retiming, applying further logic optimization to the retimed design.

13-18. (Canceled)

19.   (Previously presented)   The method of claim 4, where the prescribed period is one femtosecond or less.

20.   (Currently amended)   A method for generating timing constraints, comprising the steps of:

a step for describing a digital circuit using a hardware description language (HDL);

a step for preparing a digital circuit representation from said HDL description;

a step for removing flip-flops from said digital circuit representation and replacing said removed flip-flops with negative delay elements; and

Appl. No. 10/665,880
Amdt. dated June 17, 2009
Reply to Office Action of April 17, 2009

PATENT

a step for breaking any feedback paths in the digital circuit representation by inserting dummy flip-flops clocked by clocks all having a prescribed period **using a computer**.

21.   (Previously presented)   A computer readable storage device containing one or more programs executable by a computer to perform operations comprising:

receiving a description of a digital circuit using a hardware description language (HDL) and preparing a digital circuit representation from said HDL description;

removing flip-flops from said digital circuit representation and replacing said removed flip-flops with negative delay elements; and

breaking any feedback paths in the digital circuit representation by inserting dummy flip-flops clocked by clocks all having a prescribed period.

22.   (Previously presented)   A computer readable storage device containing one or more programs executable by a computer to perform operations comprising:

receiving a description of a digital circuit using a hardware description language (HDL) and preparing a digital circuit representation from said HDL description;

replacing flip-flops in said digital circuit representation with negative delay elements;

wherein said negative-time elements are implemented by buffers having a delay -T, where T is a delay equal to a flip-flop's clock period less a predetermined flip-flop delay;

describing a value of T using a capacitance/delay curve representing a composite of gates in a target technology library, Q pins of flip-flops in said target technology library, and a series of increasingly powerful buffer trees;

wherein said curve is first computed, then it is offset by setting a delay corresponding to a predetermined load capacitance to -T;

whereby a larger capacitive load results in a longer delay; and

whereby if a near-zero load is imposed a delay is -(T + t), where t is a (positive) difference in delay between a predetermined load and a lesser load.

Appl. No. 10/665,880
Amdt. dated June 17, 2009
Reply to Office Action of April 17, 2009

PATENT

23.   (Previously presented)   A computer driven system for generating timing constraints, comprising:

digital data storage;

coupled to the digital data storage, a digital data processor programmed to perform operations comprising:

receiving a description of a digital circuit using a hardware description language (HDL) and preparing a digital circuit representation from said HDL description;

removing flip-flops from said digital circuit representation and replacing said removed flip-flops with negative delay elements; and

breaking any feedback paths in the digital circuit representation by inserting dummy flip-flops clocked by clocks all having a prescribed period.

24.   (Previously presented)   A computer readable storage device containing one or more programs executable by a computer to perform operations comprising:

receiving a description of a digital circuit using a hardware description language (HDL) and preparing a digital circuit representation from said HDL description;

removing flip-flops from said digital circuit representation and replacing said removed flip-flops with negative delay elements; and

where some of the negative delay elements comprise buffers, said buffers having a load capacitance representing an average or weighted-average load capacitance taken over inputs of all gates and flip-flop D pins in a target technology library.

25.   (Previously presented)   A computer driven system for generating timing constraints, comprising:

digital data storage;

coupled to the digital data storage, a digital data processor programmed to perform operations comprising:

receiving a description of a digital circuit using a hardware description language (HDL) and preparing a digital circuit representation from said HDL description;

removing flip-flops from said digital circuit representation and replacing said removed flip-flops with negative delay elements; and

where some of the negative delay elements comprise buffers, said buffers having a load capacitance representing an average or weighted-average load capacitance taken over inputs of all gates and flip-flop D pins in a target technology library.